Quad Output Switching Regulator Powers Large TFT Displays

by Dongyan Zhou

Introduction

The LT1943 is a highly integrated, four-output switching regulator designed to power large TFT Liquid Crystal Displays (LCDs). The first step-down switching regulator provides a logic voltage with up to 2A of current. The other three regulators are a high-power boost regulator, a low-power boost regulator and an inverting regulator, which provide the three bias voltages, AV_{DD}, V_{ON} and V_{OFF}, required by LCDs. Switching regulators are chosen over linear regulators to accommodate a wide input voltage range (providing both step up and step down functions) and to minimize power dissipation. The LT1943's wide input range, 4.5V to 22V, allows it to accept a variety of power sources, including the commonly used 5V, 12V and 19V rails. The low-profile 28-pin TSSOP package has an exposed metal pad on the backside to maximize thermal performance.

All of the regulators are synchronized to a 1.2MHz internal clock, allowing the use of small, low cost inductors and ceramic capacitors. Since different types of panels may require different bias voltages, all output voltages are adjustable for maximum flexibility. Programmable soft-start capability is included in each of the regulators to limit inrush current.

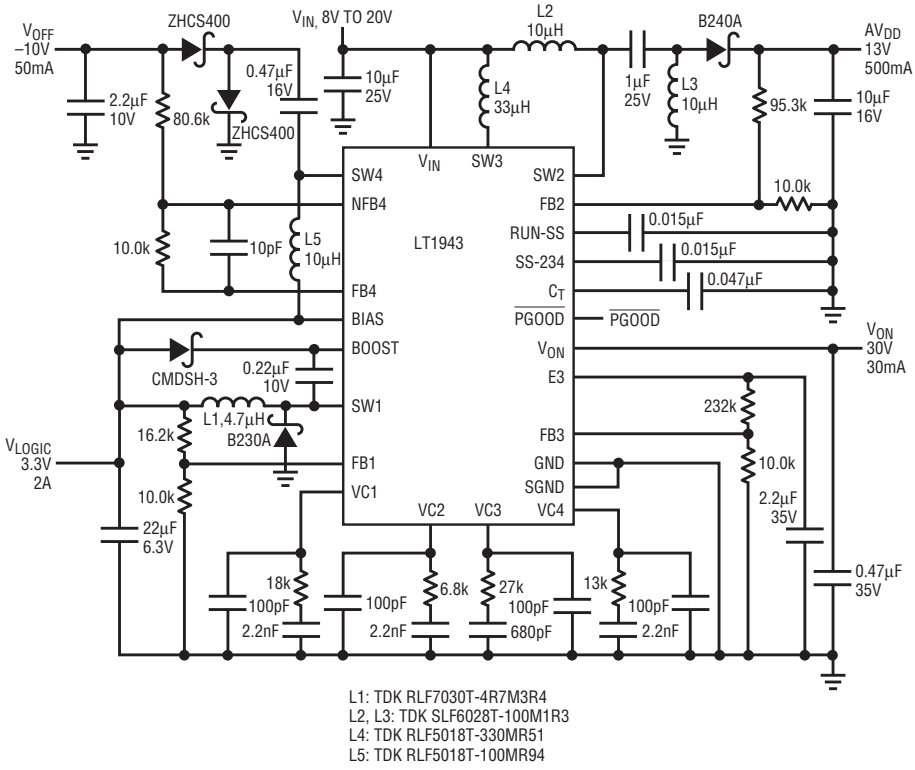

Figure 1. Quad output TFT-LCD power supply with 8V-20V input voltage range

Operation

Figure 1 shows a 4-output TFT LCD power supply with 8V to 20V input voltage range. The first output provides a 3.3V, up to 2A, logic supply using a buck regulator. The second output employs a SEPIC converter to generate a 13V, 500mA AV_{DD} bias supply. Another boost converter and an inverter generate V_{ON} and V_{OFF}.

When power is first applied to the input, the RUN-SS capacitor starts charging. When its voltage reaches 0.7V, switcher one is enabled. The capacitor at RUN-SS pin controls the ramp-rate for the Switcher 1 output, V_{LOGIC} and inrush current in L1. Switchers 2, 3 and 4 are controlled by the BIAS pin, which is usually connected to V_{LOGIC}. When the BIAS pin is higher than 2.8V, the capacitor at the SS-234 pin begins charging to enable switchers 2, 3 and 4. When AV_{DD} reaches 90% of its programmed voltage, the $\overline{PGOOD}$ pin is pulled low.

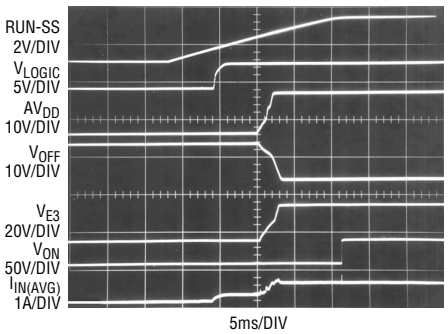

Figure 2. Startup waveforms of the power supply in Figure 1.

When AV_{DD}, V_{OFF} and E3 all reach 90% or their programmed voltages, the C_T timer is enabled and a 20µA current source begins to charge C_T. When the C_T pin reaches 1.1V, the output PNP turns on, connecting E3 to V_{ON}. Figure 2 shows the start-up sequence of the circuit in Figure 1.

If one of the regulated voltages, V_{LOGIC}, AV_{DD}, V_{OFF} or E3 dips more than 10%, the internal PNP turns off to shut down V_{ON}. This action protects the panels, as V_{ON} must be present to turn on the TFT display. Each regulator has a frequency foldback oscillator, which reduces the switching frequency to 250kHz when its FB pin is at 0V. This frequency foldback feature reduces the average inductor current during start-up and overload conditions, minimizing the power dissipation in the power switches and external components. It also helps the short-circuit protection for the Buck

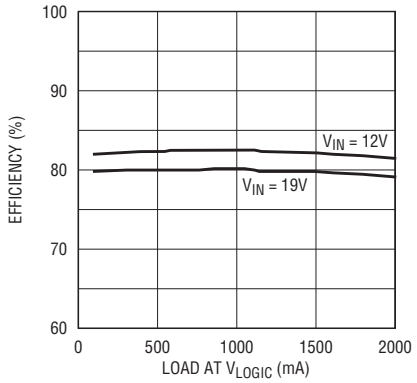

Figure 3. Total Circuit Efficiency of the power supply in Figure 1 (load at AV_{DD}: 500mA; load at V_{ON}: 30mA; load at V_{OFF}: 40mA).

and SEPIC regulators. The overall efficiency is shown in Figure 3. The converter uses all ceramic capacitors, with X5R and X7R types recommended, as these materials maintain capacitance over a wide temperature range.

If the input voltage is 5V, a boost regulator can be use in place of the SEPIC to generate the AV_{DD} supply. With the higher efficiency of the boost topology and lower input voltage, the overall circuit efficiency increases to 90%. The $\overline{PGOOD}$ pin can drive an optional PMOS device at the output of the boost regulator to disconnect the load from the input during shutdown.

Layout Considerations

Careful PC board layout is important for proper operation. Paths that carry high switching current should be short and wide to minimize parasitic inductance. In a buck regulator, this loop includes the input capacitor, internal power switch and Schottky diode. In a boost regulator, this loop includes the output capacitor, internal power switch and Schottky diode. In a SEPIC converter, this loop includes the internal power switch, flying capacitor, Schottky diode and the output capacitor. Keep all the loop compensation components and feedback resistors away from the high switching current paths. The LT1943 pinout was designed to facilitate PCB layout. Use a separate ground trace to connect the ground return of the compensation components and bottom feedback resistors to the signal ground (SGND pin). Connect the SGND to the power ground on the backside of the IC. Keep the traces from the center of the feedback resistors to the corresponding FB pins as short as possible. LT1943 has an exposed ground pad on the backside of the IC to reduce thermal resistance. A ground plane with multiple vias into ground layers should be placed underneath and near the part to conduct heat away from the IC.

Conclusion

The LT1943 provides compact power supply solutions for TFT-LCD panels. All four outputs come from switching regulators for wide input voltage range and minimum power dissipation. All four circuits use only ceramic capacitors to minimize ripple, size and cost.

LTC2904, LTC2905, LTC2906 and LTC2907 continued from page 23

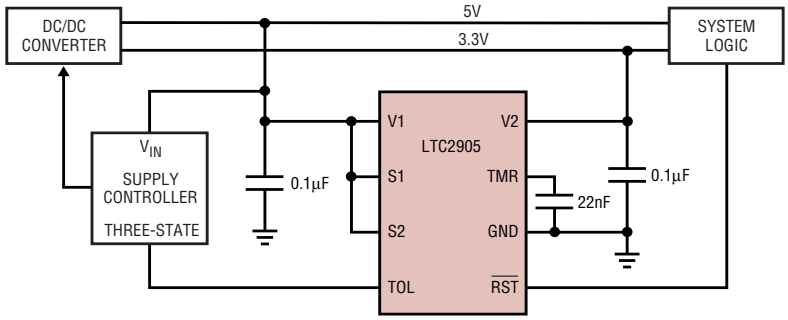

Figure 10. 5V, 3.3V dual supply monitor with voltage margining application for automated onboard testing

introduced here complement such testing in two ways.

First, a test-module can provide more supply headroom by lowering the reset trip thresholds for automated onboard testing. Using the 3-state programming input pin TOL, the global supply tolerance can be set to 5%, 7.5% or 10%. Figure 10 shows an LTC2905 used in such an application.

Second, the S1 and S2 pins can be driven by 3-state outputs for a more aggressive lowering of the trip threshold. For example, in Figure 10 the S1 and S2 pins are tied to V1 to configure the part to monitor 5V and 3.3V. If TRI-STATE buffers are added to drive the S1 and S2 pins, these pins can be set to GND during testing. Connecting S1 and S2 to GND configures the LTC2905 to monitor 2.5V and 1.8V, a significant change in trip threshold from the 5V and 3.3V thresholds respectively. During normal operation, the TRI-STATE buffers can set S1 and S2 back to V1 (High) so that the part is again configured to monitor 5V and 3.3V.

Conclusion

The LTC2904, LTC2905, LTC2906 and LTC2907 micropower dual supervisors provide the space saving, simplicity, versatility, accuracy and reliability required in a wide variety multi-voltage monitoring applications. Input supply combinations are programmable without external components. The LTC2906 and LTC2907 also include a low voltage positive adjustable threshold. The comparators are 1.5% accurate over temperature and feature built-in noise rejection. Reset state is correct for internal V_{CC} down to 1V. Reset time-out periods in the LTC2905 and LTC2907 are user adjustable with external capacitors. Power supply margining features include real-time supply tolerance and voltage threshold selections.